REMARKS

Claims 1-20 are pending and all have been rejected under either 35 U.S.C. §§ 102 or 103. In response, Applicant is amending claims 1, 9, 10, 18, and 19, and canceling claims 8 and 17, and respectfully submits that all pending claims present subject matter that is patentable over the prior art of record, and, in view of the above amendments and following remarks, requests that the Examiner reconsider the application.

OBJECTION TO THE DRAWINGS 37 CFR 1.83(a)

In paragraph 3 of the Office Action, the Examiner objected to the drawings under 37 CFR 1.83(a) because "[t]he drawings must show every feature of the invention specified in the claims." The Examiner then requested that "the following limitations must be shown or the feature(s) canceled from the claim 19 and 20: 1) an indicating means; and b) an instruction queue."

Applicant respectfully submits that Applicant is amending claim 19, which no longer includes "an indicating means." Therefore, both claims 19 and 20 have no reference to the indicating means.

However, an instruction queue 150 was shown in the FIG. 1 previously submitted. Applicant therefore respectfully requests that the Examiner withdraw the objection regarding the instruction queue.

CLAIM OBJECTIONS

In paragraph 5, the Examiner objected to claims 8, 9, 17, and 18 because "the word 'of' should be inserted between the words 'processing the'." As can be seen below, claims 8 and 17 are being canceled, and therefore the objection for these two

claims is moot. Further, Applicant is amending claims 9 and 18 to include the word "of" between the words "processing the."

REJECTIONS UNDER 35 U.S.C. § 102(b) – Smith and Pleszkun

In paragraphs 6 and 7, the Examiner rejected claims 1-9, 19, and 20 under 35 U.S.C. § 102 (b) as being anticipated by *Smith and Pleszkun*, "Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. On Comp., Vol. 37, No. 5, May 1988, pp. 562-573, (herein referred to as *Smith et al*).

Regarding claim 1, the Examiner, in paragraphs 8 and 9, asserted that *Smith et al* discloses the claimed method. The Examiner then corresponded elements of claim 1 to paragraphs of *Smith et al* that the Examiner considered corresponding to those elements of claim 1.

In response, Applicant is amending claim 1 to recite the additional feature that

> "wherein the early-retirement criteria is met when the instruction is processed to a point that continued processing of the instruction does not change the architectural state of the system processing the instruction, and, at the time of termination, the instruction has completed its function without completing its full pipeline."

Applicant respectfully submits that claim 1 is patentably distinguished from *Smith et al* for at least these added features. Throughout the paper, *Smith et al* is about *precise interrupts* (the title; col. 2, the section with heading "Classification of Interrupts", etc.). Normally, interrupts occur due to errors, exception conditions, page faults, etc. (col. 2, section A "Classification of Interrupt"), and the interrupt is *precise* if the saved process state corresponds with a sequential model of program execution where one instruction completes before the next begins (col. 1, Abstract).

In contrast, the claimed invention is about early retirement of instructions that meet the early-retirement criteria. Those early-retirement instructions, as explained in the Specification, do not have any effect on the program behavior after some stage of the pipeline, but continue to use system resources and block launching of subsequent instructions. The existence of these instructions after they have no effect on the overall state of the computation in progress can degrade system performance (page 1, lines 5-15). As claimed in claim 1, the early-retirement criteria is met when the instruction is processed to a point that continued processing of the instruction does not change the system architectural sate of the system processing the instruction. Further, as claimed, an early-completion instruction, at the time of termination, has completed its function without completing its full pipeline. As a result, the claimed invention retires or terminates an instruction "out of order of a program running the instruction" if the instruction "has met the early-retirement criteria."

In addition to the difference that *Smith et al* is about precise interrupts and the claimed invention is about early retirement of instructions, none of the paragraphs in *Smith et al* cited by the Examiner discloses, suggests, or makes obvious the above-added feature of the claimed invention. That is, none of the cited paragraph teaches that the retired instruction is processed to a point that continued processing of the instruction does not change the architectural state of the system processing the instruction, and, at the time of termination, the instruction has completed its function without completing its full pipeline. Following is the teaching in the cited paragraphs that, can be seen, do not teach, suggest, or make obvious the claimed features. For example, col. 5, paragraph 4, lines 1-7 disclose the fetch/decode pipeline, register related to the final stage of the pipeline. The cited col. 7, paragraph 4 discloses the shifting of the control information pursuant to the clock period, and the result of the functional unit is placed in the correct register. The cited col. 13, paragraph 6, lines 1-

9 disclose the future file method that uses two register files including the architectural file and the future file. The architectural file reflects the state of the architectural machine while the future file is used for computation by the functional units. The cited example 6 discloses that an instruction may finish out of order. However, as can be seen, none of the cited paragraphs disclose, suggest, or make obvious the claimed features as discussed above.

In paragraphs 22 and 23 regarding the criteria for early retirement cited in claim 8, which is now in claim 1, the Examiner asserted that "Smith et al. further discloses that the criteria for early retirement (when an instruction reaches stage 1 of the result shift register [col. 7, para.4, last 4 lines]) are met when continued processing (writing results of the instruction to correct result register [col. 7, para. 4., last 4 lines]) of the instruction does not change the architectural state (architectural file [col. 13, para. 6, lines 3-5] is changed as instructions capable of early retirement update the future file [col. 13, para. 6, lines 5-7]) of the system processing the instructions.

The cited col. 7, para. 4, last 4 lines disclose "[e]ach clock period, the control information is shifted down one stage toward stage one. When it reaches stage one, it is used during the next clock period to control the result bus so that the functional unit result is placed in the correct result register." The col.13, para. 6, lines 3-5 and 5-7 disclose "[o]ne register file reflects the state of the architectural (sequential) machine. This file will be referred to as the architectural file. A second register file is updated as soon as instructions finish and therefore runs ahead of the architectural file (i.e., it reflects the future with respect to the architectural file)." Applicant respectfully submits that Applicant's early retirement of an instruction is patentably distinguished from the teaching of these cited paragraphs for at least the reasons that there is no indication that *Smith et al's* stage one is when an instruction is retired; there is no indication that writing results of the instruction to correct result corresponds to

meeting the early-retirement criteria. Further, for the sake of argument, even if *Smith et al's* stage one is when an instruction is retired, there is no indication that after this stage one, continued execution of the retired instruction does not change the system architectural state. In fact, in *Smith et al.*, after the control information has reached stage one, it is used to control the result bus so that the functional unit is placed in the correct result register. Even though the cited paragraph 6 of col. 13 discloses a register file that reflects the state of the architectural machine, there is no teaching that, at the time of termination, continued processing of a retired instruction does not change the system architectural state.

Because claim 1 recites limitations patentably distinguished from *Smith et al*, claim 1 is patentable.

Claims 2-7 and 9 depend directly or indirectly from claim 1 and are therefore patentable for at least the same reasons as claim 1. Claims 2-7 and 9 are also patentable for their additional limitations.

Claim 10 recites limitations corresponding to claim 1, and is therefore patentable for at least the same reasons as claim 1. Claims 11-16 and 18 depend directly or indirectly from claim 10 and are therefore patentable for at least the same reasons as claim 1. Claims 11-16 and 18 are also patentable for their additional limitations.

Claim 19 recites limitations corresponding to claim 1, and is therefore patentable for at least the same reasons as claim 1. Claim 20 depends directly from claim 19 and is therefore patentable for at least the same reasons as claim 19. Claim 19 is also patentable for its additional limitations.

In paragraphs 10-25, 28, and 29, the Examiner discussed reasons for rejecting dependent claims. However, because dependent claims are patentable for at least the same reasons as the independent claims from which the dependent claims depend,

Applicant, without responding to the Examiner's assertions regarding the dependent claims, wishes to reserve the rights to respond to those assertions at a later time as appropriate.

REJECTIONS UNDER 35 U.S.C. § 103(a) – Smith et al in view of Tannenbaum

In paragraphs 30-36, the Examiner rejected claims 10-18.

In paragraph 31, the Examiner rejected claims 10-18 under 35 U.S.C. § 103(a) for the same reasons as claims 1-9 as being unpatentable over *Smith et al* in view of *Tannenbaum*, "Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12 (herein referred to as *Tannenbaum*).

In paragraphs 32-36, the Examiner asserted that *Smith et al* teaches the claimed elements of claims 10-18 as detailed in the rejection of claims 1-9. However, the Examiner conceded that *Smith et al* differs from Applicant's invention in that *Smith et al* does not teach that instructions on a computer-readable medium embodying instructions that cause a computer to perform the limitations of claims 10-18 of Applicant's invention. The Examiner then continued that *Tannenbaum* teaches that any instruction executed by hardware can also be simulated in software (pg 11, para. 4, lines 1-2) and that hardware is generally immutable (first para. after sec 1.4 header) while software allows for more rapid change (pg. 11, para. 4, lines 2-4). The Examiner then concluded "it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Smith et al. processor by converting it to instructions on a machine-readable medium."

As discussed above, *Smith et al* does not teach, suggest, or make obvious the cited feature "wherein the early retirement criteria is met when the instruction is processed to a point that continued processing of the instruction does not change the architectural state of the system processing the instruction, and, at the time of

termination, the instruction has completed its function without completing its full pipeline." Applicant respectfully submits that the cited paragraphs of *Tannenbaum* do not provide this claimed feature, either. As a result, claim 10 is patentable over *Smith et al* and *Tannenbaum*, either alone or in combination.

Claims 11-16 and 18 depend directly or indirectly from claim 10 and are therefore patentable for at least the same reasons as claim 10. Claims 11-16 and 18 are also patentable for their additional limitations as appropriate.

SUMMARY

In conclusion, Applicant respectfully submits that pending claims 1-7, 9-16, and 18-20 clearly present subject matter that is patentable over the prior art of record, and therefore requests that the Examiner withdraw the rejections of the pending claims and pass the application to issue. If the Examiner has questions regarding this case, the Examiner is invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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